REMARKS

I.   INTRODUCTION

Claims 1-36 and 49 are currently pending.

II.   ELECTION / RESTRICTIONS UNDER 37 C.F.R. § 1.142

Claim 49 stands withdrawn from consideration as being directed to a non-elected invention.

Claim 49 is similar to claim 1, but is written in Means Plus Function format. See MPEP 2181 and 35 U.S.C. § 112 ¶ 6. Claim 49 replaces the detecting, calculating and correcting language from claim 1 with a means for detecting, means for calculating and a means for correcting.

In view of the above, it is respectfully submitted that claim 49 is not independent or distinct from the invention as claimed in the currently amended claim 1 and no election/restriction should apply.

III.   REJECTION UNDER 35 U.S.C. § 102

Claims 1-2, 4-8, 11-13, 15 and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Leedy (US 5,103,557).

The Examiner states that Leedy discloses "a modified net list used to form interconnect patterns." Applicant respectfully disagrees that Leedy presents all the elements of claim 1 as required for anticipation under 35 U.S.C. § 102. Claim 1 recites "calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data." See Claim 1 and, for example, page 11, lines 2-6, of the application.

Leedy, on the other hand, uses a tester surface to bring a wafer within a few mils of said tester surface using the pressure of a fluid, separating the tester surface and the wafer, and makes a first approximation of the contact points through a conventional optical aligner. See column 4, line 66 through column 5, line 11, of Leedy. The alignments are determined by using alignment patterns in predetermined positions on both the wafer being tested and the tester surface. See column 5, lines 3-7, of Leedy. The data from the Leedy invention lists the location

of the defective transistors or ICLUs. See column 5, lines 33-35, of Leedy. The CAD means then works out an interconnect strategy, forming a net list of interconnect patterns to bypass defective ICLUs by interconnecting defect-free ICLUs from a stock of redundant ICLUs. See column 5, lines 37-43, of Leedy.

Conversely, the present invention as recited in amended claim 1 calculates the *displacement* between the design position and the actual position of the component. See Claim 1 and, for example, page 11, lines 2-6, of the application. Leedy only lists the *location* of defective transistors or ICLUs. See column 5, lines 33-35, of Leedy. Because Leedy only determines which transistors and ICLUs are not accurately aligned per the CAD master placement scheme and interconnects redundant ICLUs to replace them, it never determines the displacement between the design position and the actual location of the component. See column 5, lines 3-43, of Leedy. Thus, Leedy does not disclose the present invention as recited, for example, in claim 1.

Examiner stated in his response to arguments that Leedy discloses using a modified net list to form interconnect patterns, the process involving depositing a layer of insulation over the wafer surface and metal deposited vias to connect with the underlying electrical components formed under the insulation layer. Independent claim 1, on the other hand, recites "correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component." See Claim 1 and, for example, page 11, lines 2-5, page 14, lines 16-35, and Figs. 7 and 8, of the application.

As argued above, Leedy calculates the location of defective transistors and ICLUs and interconnects redundant ICLUs to replace said defective ICLUs. See column 5, lines 3-43, of Leedy. Because Leedy never calculates the displacement between design data and the actual location of a component, it cannot make corrections based on displacement data. In fact, the word "displacement" never appears in Leedy.

The above comments are specifically directed to claim 1. However, it is respectfully submitted that the comments would be helpful in understanding various differences of various other claims over the cited reference.

In view of the above, it is respectfully submitted that the rejection is overcome.

IV.   REJECTION UNDER 35 U.S.C. § 103

Claims 19-20, 22-26 and 29-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leedy (US 5,103,557) in view of Kulkarni et al (US 5,991,699).

Claim 19 discloses "calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component detected from first image data obtained by imaging the surface of said board, and holding said displacement as first displacement data." See Claim 19 and, for example, page 11, lines 2-6, of the application. Per the above, Leedy fails to disclose calculating the displacement between the design position and the actual position of a component.

The above comments are specifically directed to claim 19. However, it is respectfully submitted that the comments would be helpful in understanding various differences of various other claims over the cited reference.

In view of the above, it is respectfully submitted that the rejection is overcome.

Claims 14, 16 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leedy (US 5,103,557) in view of Kulkarni et al (US 5,991,699).

Claims 14, 16 and 18 depend either directly or indirectly from claim 1, adding further limitations thereto. Per the above, Leedy fails to disclose calculating the displacement between the design position and the actual position of a component.

In view of the above, it is respectfully submitted that the rejection is overcome.
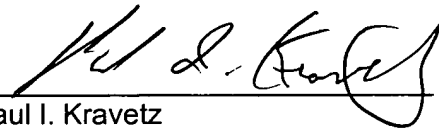
V.   CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An action to that effect is courteously solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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